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1 [Symbolic transfer function-based approaches to certified compilation](#)
[Xavier Rival](#)

 January 2004 **POPL '04: Proceedings of the 31st ACM SIGPLAN-SIGACT symposium on Programming Languages**
Publisher: ACM

 Full text available: [Pdf](#) (212.73 KB) [Additional Information: full citation, abstract, ...](#)
Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 46, Citation (

We present a framework for the certification of compilation and of compilation. It uses a symbolic transfer functions-based representation of programs, so that compiled programs present similar behaviors. This checking ...

Keywords: abstract interpretation, certification, compilation, static analysis

Also published in:

 January 2004 **SIGPLAN Notices** Volume 39 Issue 1

2 [The design and development of ZPL](#)
[Lawrence Snyder](#)

 June 2007 **HOPL III: Proceedings of the third ACM SIGPLAN conference on Compiler Construction**
Publisher: ACM

 Full text available: [Mov](#) (56:16 MIN), [Pdf](#) (2.65 MB) [Additional Information: full citation, abstract, ...](#)
Bibliometrics: Downloads (6 Weeks): 20, Downloads (12 Months): 197, Citation (

ZPL is an implicitly parallel programming language, which means all instructions to manage the parallelism are inserted by the compiler. It is the first implicitly parallel programming language that provides performance portability, that is, consistent ...

Keywords: CTA, WYSIWYG performance model, parallel language design, problem space promotion, regions, type architecture

3 [Parallelizing load/stores on dual-bank memory embedded processor](#)
[Xiaotong Zhuang, Santosh Pande](#)


 August 2006 **Transactions on Embedded Computing Systems (TECS)** ,

Publisher: ACM

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Bibliometrics: Downloads (6 Weeks): 9, Downloads (12 Months): 59, Citation (



Many modern embedded processors such as DSPs support partitioned memory (e.g., cache or dual-bank memory) along with parallel load/store instructions to improve throughput and performance. In order to effectively utilize the ...

Keywords: DSP architectures, memory bank allocation, parallel load/st

4 [Communications of the ACM: Volume 52 Issue 4](#)


 April 2009 [Communications of the ACM](#)

Publisher: ACM

Full text available:  [Digital Edition](#),  [Pdf](#) (7.58 MB) Additional Information: [full citation](#), [abstract](#), [...](#)

Bibliometrics: Downloads (6 Weeks): 3709, Downloads (12 Months): 3709, Cit

5 [Inter-cluster communication in VLIW architectures](#)

 A. S. Terechko, H. Corporaal

June 2007 [Transactions on Architecture and Code Optimization \(TA](#)

Publisher: ACM


Full text available:  [Pdf](#) (996.47 KB) Additional Information: [full citation](#), [abstract](#), [...](#)

Bibliometrics: Downloads (6 Weeks): 24, Downloads (12 Months): 162, Citatio

The traditional VLIW (very long instruction word) architecture with a single long instruction word does not scale up well to address growing performance demands on embedded media processors. This paper presents a VLIW processor in smaller clusters, which are ...


Keywords: Instruction-level parallelism, VLIW, clock frequency, cluster scheduler, intercluster communication, optimizing compiler, pipelining, i

6 [Reducing the cost of conditional transfers of control by using compact instructions](#)

 William Krehling, Stephen Hines, David Whalley, Gary Tyson

July 2006 [LCTES '06: Proceedings of the 2006 ACM SIGPLAN/SIGBED conference on Languages, Compilers, and Tool Support for Embedded Systems](#)

Publisher: ACM

Full text available:  [Pdf](#) (124.43 KB) Additional Information: [full citation](#), [abstract](#), [...](#)

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 21, Citation (

A significant portion of a program's execution cycles are typically dedicated to conditional transfers of control. Much of the research on reducing the costs of these transfers has been largely ...

Keywords: branch, comparison, compiler, optimization

Also published in:







July 2006 [SIGPLAN Notices](#) Volume 41 Issue 7



7 [Handling irreducible loops: optimized node splitting versus DJ-graph](#)

-  [Sebastian Unger, Frank Mueller](#)
 July 2002 **Transactions on Programming Languages and Systems (**
Publisher: ACM
 Full text available:  [Pdf](#) (386.11 KB) Additional Information: [full citation](#), [abstract](#), [bibliometrics](#)
Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 52, Citation (

This paper addresses the question of how to handle irreducible regions (become even more relevant for contemporary processors since recent V rely on instruction scheduling. The contributions ...


Keywords: Code optimization, compilation, control flow graphs, instruction flowgraphs, loops, node splitting, reducible flowgraphs

- 8 [Communications of the ACM: Volume 51 Issue 12](#)
 December 2008 Communications of the ACM
Publisher: ACM
 Full text available:  [Digital Edition](#) ,  [Pdf](#) (6.91 MB) Additional Information: [full citation](#)
Bibliometrics: Downloads (6 Weeks): 1165, Downloads (12 Months): 3218, Cit
- 9 [Communications of the ACM: Volume 52 Issue 2](#)
 February 2009 Communications of the ACM
Publisher: ACM
 Full text available:  [Digital Edition](#) ,  [Pdf](#) (7.09 MB) Additional Information: [full citation](#)
Bibliometrics: Downloads (6 Weeks): 1895, Downloads (12 Months): 4766, Cit


- 10 [Fast online pointer analysis](#)
 [Martin Hirzel, Daniel Von Dincklage, Amer Diwan, Michael Hind](#)
 April 2007 **Transactions on Programming Languages and Systems (**
Publisher: ACM
 Full text available:  [Pdf](#) (430.96 KB) Additional Information: [full citation](#), [abstract](#), [bibliometrics](#)
Bibliometrics: Downloads (6 Weeks): 16, Downloads (12 Months): 160, Citation (

Pointer analysis benefits many useful clients, such as compiler optimization. Unfortunately, common programming language features such as dynamic language interfaces, make pointer analysis difficult. ...


Keywords: Pointer analysis, class loading, native interface, reflection

- 11 [Exhaustive Optimization Phase Order Space Exploration](#)
[Prasad A. Kulkarni, David B. Whalley, Gary S. Tyson, Jack W. Davidson](#)
 March 2006 **CGO '06: Proceedings of the International Symposium on Code**
Publisher: IEEE Computer Society
 Full text available:  [Pdf](#) (400.93 KB) Additional Information: [full citation](#), [abstract](#), [bibliometrics](#)
Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 42, Citation (


The phase-ordering problem is a long standing issue for compiler writers: typically have numerous different code-improving phases, many of which. These phases interact by enabling or disabling opportunities ...

12 [A new viewpoint on code generation for directed acyclic graphs](#) [S. Liao, K. Keutzer, S. Tjiang, S. Devadas](#)January 1998 **Transactions on Design Automation of Electronic Systems****Publisher:** ACMFull text available:  [Pdf](#) (661.59 KB)Additional Information: [full citation](#), [abstract](#), [bibliometrics](#)**Bibliometrics:** Downloads (6 Weeks): 6, Downloads (12 Months): 46, Citation (

We present a new viewpoint on code generation for directed acyclic graphs based on binate covering, the problem of satisfying, with minimum cost and can take into account commutativity ...

Keywords: binate covering, code generation, directed acyclic graphs**13** [A text-compression-based method for code size minimization in embedded systems](#) [Stan Liao, Srinivas Devadas, Kurt Keutzer](#)January 1999 **Transactions on Design Automation of Electronic Systems****Publisher:** ACMFull text available:  [Pdf](#) (184.16 KB)Additional Information: [full citation](#), [abstract](#), [bibliometrics](#)**Bibliometrics:** Downloads (6 Weeks): 4, Downloads (12 Months): 32, Citation (


We address the problem of code-size minimization in VLSI systems with embedded systems. Reducing code size reduces the production cost of embedded systems. We develop code-size minimization strategies. In our framework, ...

Keywords: code size optimization, compression**14** [Energy aware compilation for DSPs with SIMD instructions](#) [Markus Lorenz, Lars Wehmeyer, Thorsten Dräger](#)July 2002 **LCTES/ SCOPES '02: Proceedings of the joint conference on Languages, Compilers, and Tools for Embedded Systems: software and compilers for embedded systems****Publisher:** ACMFull text available:  [Pdf](#) (220.77 KB)Additional Information: [full citation](#), [abstract](#), [bibliometrics](#)**Bibliometrics:** Downloads (6 Weeks): 6, Downloads (12 Months): 55, Citation (

The growing use of digital signal processors (DSPs) in embedded systems is driving the need for optimizing compilers supporting special hardware features. In this paper, we present code size optimizations with the aim of minimizing energy consumption of ...

Keywords: DSP, SIMD instruction, energy minimization, vectorization,

Also published in:

July 2002 **SIGPLAN Notices** Volume 37 Issue 7**15** [Efficient software implementation of embedded communication protocols](#) [asynchronous software thread integration with time- and space-efficient](#)[Nagendra J. Kumar, Vasanth Asokan, Siddhartha Shivshankar, Alexander C](#)February 2007 **Transactions on Embedded Computing Systems (TECS)****Publisher:** ACM



Full text available:  Pdf (596.75 KB)Additional Information: [full citation](#), [abstract](#), [terms](#)**Bibliometrics:** Downloads (6 Weeks): 10, Downloads (12 Months): 130, Citation (

The overhead of context switching limits efficient scheduling of multiple uniprocessor when real-time requirements exist. A software-implemented communication protocol crippled by this problem. The available idle time may ...

Keywords: Asynchronous software thread integration, J1850, fine-grain software migration, software-implemented communication protocol conf


16 [Hardware/Software Design Space Exploration for a Reconfigurable F](#)
[Alberto La Rosa, Luciano Lavagno, Claudio Passerone](#)

March 2003 **DATE '03: Proceedings of the conference on Design, Auto**
Volume 1, Volume 1

Publisher: IEEE Computer SocietyFull text available:  Publisher Site,  Pdf (103.11 KB) Additional Information: [full citation](#), [abstract](#), [terms](#)**Bibliometrics:** Downloads (6 Weeks): 0, Downloads (12 Months): 25, Citation (

This paper describes an approach to hardware/software design space ex processors. The existing compiler tool-chain, because of the user-defina extended in order to offer developers an easy way ...

17 [Asynchronous software thread integration for efficient software](#)

 [Nagendra J. Kumar, Siddhartha Shivshankar, Alexander G. Dean](#)

July 2004 **LCTES '04: Proceedings of the 2004 ACM SIGPLAN/SIGBED co**
 compilers, and tools for embedded systems

Publisher: ACMFull text available:  Pdf (229.95 KB) Additional Information: [full citation](#), [abstract](#), [terms](#)**Bibliometrics:** Downloads (6 Weeks): 3, Downloads (12 Months): 60, Citation (

The overhead of context-switching limits efficient scheduling of multiple uniprocessor when real-time requirements exist. Existing software three reduce context switches, but only provide synchronous ...

Keywords: J1850, asynchronous software thread integration, fine-grain software migration, software-implemented communication protocol conf

Also published in:

July 2004 **SIGPLAN Notices** Volume 39 Issue 7

18 [Synthesis of concurrent system interface modules with automatic pro](#)
[Bill Lin, Steven Vercouteren](#)

November 1994 **ICCAD '94: Proceedings of the 1994 IEEE/ACM internation**
 design

Publisher: IEEE Computer Society PressFull text available:  Pdf (1.04 MB) Additional Information: [full citation](#), [abstract](#), [terms](#)**Bibliometrics:** Downloads (6 Weeks): 2, Downloads (12 Months): 11, Citation (

We describe a new high-level compiler called Integral for designing syst
is a high-level concurrent algorithmic specification that can model comp
logical and arithmetic computations, ...

19 [Pointer analysis for structured parallel programs](#)



Radu Rugina, Martin C. Rinard

January 2003 **Transactions on Programming Languages and Systems**

Publisher: ACM

Full text available: Pdf (383.29 KB)

Additional Information: [full citation](#), [abstract](#), ...

Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 86, Citation

This paper presents a novel interprocedural, flow-sensitive, and context
algorithm for multithreaded programs that may concurrently update sh
designed to handle programs with structured parallel ...

Keywords: Pointer analysis

20 [Proceedings of the 2009 Conference on Asia and South Pacific Desi](#)

Kazutoshi Wakabayashi

January 2009 **ASP-DAC '09: Proceedings of the 2009 Conference on Asia a**
Automation

Publisher: IEEE Press

Additional Information: [full citation](#), [abstract](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citatio

On behalf of the Organizing Committee, I would like to invite you to att
Design Automation Conference 2009 (ASP-DAC 2009), being held here
from January 19 through 22, 2009, jointly with the Electronic ...

Re:

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